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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,561	02/29/2000	NOBUAKI HASHIMOTO	105030	8576

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	09/486,561	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	David A. Zarneke	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-8,11,12,14-16 and 21-26* is/are pending in the application.

4a) Of the above claim(s) *1,2,5-7 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,11,12,14-16,21,22 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/24/04 with respect to the rejection of claims 8, 11, 12, 14-16, 21 and 22 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

Claims 1, 2, 5-8, 11, 12, 14-16 and 21-26 are pending and claims 1, 2, 5-7, and 23 have been withdrawn from consideration. Leaving claims 8,11,12,14-16,21 and 22, 24-26 as the examined claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8, 14-16, 21, 22, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, US Patent 6,077,382, in view of Maeta et al., US Patent 5,677,246.

Watanabe teaches a semiconductor device, comprising:

a semiconductor chip having electrodes;

a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via at least part of said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers substantially all area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed (figures 1-4, 4-4, 6, &/or 7-4).

Watanabe, which teaches the adhesive covers **substantially** all, fails to teach the adhesive covers **all** area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed.

Maeta teaches a chip attached to a substrate using an adhesive wherein the adhesive covers all of the lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed (Figure 11).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the adhesive of Maeta in the invention of Watanabe because the adhesive of Maeta teaches that an adhesive that covers all the side surfaces of the chip firmly secures the chip to the substrate, protects the chip from internal stress caused by heat and physical stress, and the chip is less liable to be affected by the external environment and impact, which improves chip reliability (17, 11+).

Though Maeta uses a nonconductive adhesive, the benefits taught by Maeta would apply and be beneficial when using a conductive adhesive, as in the present invention.

Regarding claims 16, 21 and 22, Watanabe teaches at least a part of said adhesive having a thickness substantially the same as said semiconductor chip. In teaching the side surfaces of the chip are substantially covered, Watanabe inherently teaches **at least part** of the adhesive as being substantially as thick as the chip.

With respect to claims 24-26, the combination of Watanabe and Maeta teaches a part of said adhesive covering substantially all area of said lateral surfaces of said semiconductor chip has part of said conductive particles dispersed therein.

As above, the benefits taught by Maeta of depositing a nonconductive adhesive such that all lateral surfaces of the chip are covered would be greatly beneficial when using a conductive adhesive.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, US Patent 6,077,382, in view of Maeta et al., US Patent 5,677,246, as applied to claim 8 above, and further in view of Tsukagoshi et al., US Patent 5,804,882.

Watanabe and Maeta fail to teach the adhesive as being provided to cover said interconnect pattern in its entirety.

Tsukagoshi teaches an adhesive having conductive particles dispersed therein wherein the adhesive as being provided to cover said interconnect pattern in its entirety (Figures 1-4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the adhesive coverage of Tsukagoshi in the invention of Watanabe because it is merely a matter an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). A skilled artisan would know to cover the entire interconnect pattern because it would ensure a complete electrical connection between the chip and the substrate.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, US Patent 6,077,382, in view of Maeta et al., US Patent 5,677,246, as applied to claim 8 above, and further in view of Canning et al., US Patent 5,783,465.

Watanabe and Maeta fail to teach the adhesive as including a shading material.

Canning teaches adding a pigment material (shading material) to an ACF film (5, 14+).

It would have been obvious to one of ordinary skill in the art to use the pigment of Canning in the invention of Watanabe because Canning teaches the conventionality of using a pigment in an ACF film. Pigments, or shading materials, are useful in films to provide color to the film or to reflect light away from sensitive materials.

The use of conventional materials to perform there known functions in a conventional process is obvious (*In re Aller* 220 F.2d 454,456,105 USPQ 233,235 (CCPA 1955)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
February 16, 2005